CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of forming bitline contacts, the method comprising:

forming gate conductor lines with a capping layer on a substrate;

depositing an oxide layer over the capping layer;

forming a bitline contact line mask over portions of the oxide layer;

etching the bitline contact line mask to the capping layer and between the gate conductor lines stopping at the substrate;

depositing a silicon layer on the substrate between the conductor lines and non etched portions of the oxide layer;

depositing a bitline layer on the silicon layer;

masking and etching portions of the bitline layer; and

depositing metal over the silicon layer and on sides of non etched portions of the bitline layer to form left and right bitlines.

2. The method of claim 1, wherein a layer of BoroPhosphoSilicate Glass (BPSG) is deposited over the capping layer prior to the deposition of the oxide layer.

3. The method of claim 2, further comprising annealing the BPSG layer.

4. The method of claim 3, further comprising planarizing the BPSG layer to below tops of the gate conductor lines.

5. The method of claim 1, wherein the oxide layer is a TEOS layer.

6. The method of claim 5, further comprising planarizing the TEOS layer prior to forming the bitline contact line mask.

7. The method of claim 1, further comprising forming spacers between adjacent gate conductor lines.

8. The method of claim 7, further comprising depositing a layer of BoroPhosphoSilicate Glass (BPSG) over the capping layer wherein the etching of the oxide and BPSG selective to the capping layer

and selective to the spacers.

9. The method of claim 1, wherein the silicon layer is an n+ amorphous/polysilicon layer.

10. The method of claim 9, wherein the n+ amorphous/polysilicon layer is selectively etched or polished back to the oxide layer, the oxide layer being a TEOS layer.

11. The method of claim 10, further comprising etching the n+ amorphous/polysilicon layer to below tops of the gate conductor lines and below the oxide layer.

12. The method of claim 11, further comprising planarizing the bitline layer, the bitline layer being a TEOS layer.

13. The method of claim 1, wherein the etching of the bitline stops at the non etched portions of the oxide layer.

14. The method of claim 1, wherein the oxide layer is etched to the silicon layer selective to the capping layer encapsulating the gate conductor lines.

15. The method of claim 1, further comprising forming insulating sidewalls on the gate conductor lines.

16. The method of claim 15, wherein the insulating materials is silicon nitride.

17. The method claim 16, further comprising depositing a conformal silicon nitride layer on the gate conductor lines and active areas and isolation areas between the active areas.

18. The method of claim 1, wherein an isotropic dry etch is used to recess the silicon layer to below a level of the capping layer.

19. A bitline contact for a vertical DRAM array, comprising:

gate conductor lines formed on a substrate;

a polysilicon layer formed between the gate conductor lines;

an oxide layer formed over at least one of the gate conductor lines; and

metal formed over the gate conductor lines on opposing sides of the oxide layer thereby forming a left bitline and a right bitline, wherein the left

and right bitlines are vertically non-twisted between bitline levels.

20. The bitline contact of claim 19, further comprising an insulator layer formed between the gate conductor lines and the polysilicon layer.

21. The bitline contact of claim 19, wherein the polysilicon layer is an N+ amorphous/polycrystalline silicon layer.

22. The bitline contact of claim 19, wherein the oxide layer is a TEOS oxide.

23. The bitline contact of claim 19, further comprising spacers between two adjacent gate conductor lines of the gate conductor lines.

24. The bitline contact of claim 23, further comprising a layer of BoroPhosphoSilicate Glass (BPSG) and a topping oxide layer formed over the spacers.

25. The bitline contact of claim 24, wherein the left and right bitlines are formed partially over the topping oxide layer.

26. The bitline contact of claim 24, wherein the topping oxide layer is a TEOS layer.

27. The bitline contact of claim 19, wherein the polysilicon layer is formed below tops of the gate conductor lines.

28. The bitline contact of claim 27, wherein the right and left bitlines are partially formed below the tops of the gate conductor lines.